Amendments to the Claims:

Claims 1-162 (canceled)

163. (currently amended) A chip package comprising:

a first ~~polymer~~ insulating layer;

a die between a first portion of said first ~~polymer~~ insulating layer and a second portion of said first ~~polymer~~ insulating layer, wherein said die has a top surface substantially coplanar with a top surface of said first portion and with a top surface of said second portion;

a second ~~polymer~~ insulating layer on said top surface of said die and on said top surfaces of said first and second portions;

a first patterned metal layer over said second ~~polymer~~ insulating layer, over said top surface of said die and over said top surfaces of said first and second portions, wherein said first patterned metal layer is connected to said die through an opening in said second ~~polymer~~ insulating layer, and wherein said first patterned metal layer comprises electroplated copper; ~~, and wherein said first patterned metal layer comprises at least a part of a passive device comprising a portion directly over said top surface of said first portion;~~

a passive device over said second insulating layer, wherein said passive device comprises a portion directly over said top surface of said first portion;

a third ~~polymer~~ insulating layer on said first patterned metal layer, on said passive device, over said second ~~polymer~~ insulating layer, over said top surface of said die and over said top surfaces of said first and second portions; and

a metal bump directly over said top surface of said first portion, wherein said metal bump is connected to said die through said first patterned metal layer.

164. (previously presented) The chip package in claim 163, wherein said passive device comprises a resistor.

165. (previously presented) The chip package in claim 163, wherein said passive device comprises a capacitor.

166. (currently amended) The chip package in claim 163, wherein said second ~~polymer~~ insulating layer comprises polyimide.

167. (currently amended) The chip package in claim 163, wherein said second ~~polymer~~ insulating layer comprises benzocyclobutene (BCB).

168. (currently amended) The chip package in claim 163 further comprising a second patterned metal layer on said third ~~polymer~~ insulating layer, over said top surface of said die and over said top surfaces of said first and second portions, wherein said second patterned metal layer comprises electroplated copper, wherein said second patterned metal layer is connected to said first patterned metal layer through an opening in said third ~~polymer~~ insulating layer, and wherein said metal bump is connected to said first patterned metal layer through said second patterned metal layer.

169. (currently amended) The chip package in claim 163, wherein said third ~~polymer~~ insulating layer comprises polyimide.

170. (currently amended) The chip package in claim 163, wherein said third ~~polymer~~ insulating layer comprises benzocyclobutene (BCB).

171. (previously presented) The chip package in claim 163, wherein said metal bump comprises a solder.

172. (previously presented) The chip package in claim 163, wherein said passive device comprises an inductor.

173. (previously presented) The chip package in claim 163, wherein said metal bump

comprises gold.

174. (previously presented) The chip package in claim 163, wherein said passive device comprises a waveguide.

175. (previously presented) The chip package in claim 163, wherein said passive device comprises a filter.

176. (previously presented) The chip package in claim 163 further comprising a substrate under said die and under said first and second portions.

177. (previously presented) The chip package in claim 176, wherein said substrate comprises silicon.

178. (currently amended) The chip package in claim 163, wherein said first ~~polymer~~ insulating layer comprises an epoxy.

179. (currently amended) A chip package comprising:

a first ~~polymer~~ insulating layer;

a die between a first portion of said first ~~polymer~~ insulating layer and a second portion of said first ~~polymer~~ insulating layer, wherein said die has a top surface substantially coplanar with a top surface of said first portion and with a top surface of said second portion;

a second ~~polymer~~ insulating layer on said top surface of said die and on said top surfaces of said first and second portions;

a patterned metal layer over said second ~~polymer~~ insulating layer, over said top surface of said die and over said top surfaces of said first and second portions, wherein said patterned metal layer is connected to a first metal pad of said die through a first opening in said second ~~polymer~~ insulating layer, and to a second metal pad of said die through a second opening in said second ~~polymer~~ insulating layer, wherein said first

metal pad is connected to said second metal pad through said patterned metal layer; and

a metal bump directly over said top surface of said first portion, wherein said metal bump is connected to said die through said patterned metal layer.

180. (currently amended) The chip package in claim 179, wherein said first ~~polymer~~ insulating layer comprises an epoxy.

181. (previously presented) The chip package in claim 179, wherein said metal bump comprises a solder.

182. (currently amended) The chip package in claim 179, wherein said second ~~polymer~~ insulating layer comprises polyimide.

183. (currently amended) The chip package in claim 179, wherein said second ~~polymer~~ insulating layer comprises benzocyclobutene (BCB).

184. (currently amended) The chip package in claim 179 further comprising a third ~~polymer~~ insulating layer on said patterned metal layer, over said second ~~polymer~~ insulating layer, over said top surface of said die and over said top surfaces of said first and second portions.

185. (currently amended) The chip package in claim 184, wherein said third ~~polymer~~ insulating layer comprises polyimide.

186. (currently amended) The chip package in claim 184, wherein said third ~~polymer~~ insulating layer comprises benzocyclobutene (BCB).

187. (currently amended) The chip package in claim 179, wherein said patterned metal layer comprises a ground bus connecting said first metal pad to ~~and~~ said second metal

pad. ~~pads through said first and second openings.~~

188. (currently amended) The chip package in claim 179, wherein said patterned metal layer comprises a power bus connecting said first metal pad to ~~and~~ said second metal pad. ~~pads through said first and second openings.~~

189. (currently amended) The chip package in claim 179, wherein said patterned metal layer comprises a signal trace connecting said first metal pad to ~~and~~ said second metal pad. ~~pads through said first and second openings.~~

190. (currently amended) The chip package in claim 179 further comprising a filter ~~passive device~~ over said second ~~polymer~~ insulating layer.

191. (currently amended) The chip package in claim 179 ~~190,~~ further comprising ~~wherein said passive device comprises~~ an inductor over said second ~~polymer~~ insulating layer.

192. (currently amended) The chip package in claim 179 ~~190,~~ further comprising ~~wherein said passive device comprises~~ a capacitor over said second ~~polymer~~ insulating layer.

193. (currently amended) The chip package in claim 179 ~~190,~~ further comprising ~~wherein said passive device comprises~~ a resistor over said second ~~polymer~~ insulating layer.

194. (previously presented) The chip package in claim 179 further comprising a substrate under said die and under said first and second portions.

195. (previously presented) The chip package in claim 194, wherein said substrate comprises silicon.

196. (previously presented) The chip package in claim 179, wherein said patterned metal layer comprises electroplated copper.

197. (currently amended) A chip package comprising:

a first ~~polymer~~ insulating layer;

a die between a first portion of said first ~~polymer~~ insulating layer and a second portion of said first ~~polymer~~ insulating layer, wherein said die has a top surface substantially coplanar with a top surface of said first portion and with a top surface of said second portion;

a second ~~polymer~~ insulating layer on said top surface of said die and on said top surfaces of said first and second portions;

a patterned metal layer over said second ~~polymer~~ insulating layer, over said top surface of said die and over said top surfaces of said first and second portions, wherein said patterned metal layer comprises electroplated copper, and wherein said patterned metal layer comprises a ground bus connected to a first metal pad of said die through a first opening in said second ~~polymer~~ insulating layer, and to a second metal pad of said die through a second opening in said second ~~polymer~~ insulating layer, wherein said first metal pad is connected to said second metal pad through said ground bus; and

a metal bump directly over said top surface of said first portion, wherein said metal bump is connected to said die through said patterned metal layer.

198. (currently amended) The chip package in claim 197 further comprising an inductor over said second ~~polymer~~ insulating layer.

199. (currently amended) The chip package in claim 197 further comprising a resistor over said second ~~polymer~~ insulating layer.

200. (currently amended) The chip package in claim 197, wherein said first ~~polymer~~

insulating layer comprises an epoxy.

201. (currently amended) The chip package in claim 197 further comprising a capacitor over said second ~~polymer~~ insulating layer.

202. (currently amended) The chip package in claim 197, wherein said second ~~polymer~~ insulating layer comprises polyimide.

203. (currently amended) The chip package in claim 197 further comprising a third ~~polymer~~ insulating layer on said patterned metal layer.

204. (currently amended) The chip package in claim 197, wherein said second ~~polymer~~ insulating layer comprises benzocyclobutene (BCB).

205. (previously presented) The chip package in claim 197, wherein said metal bump comprises a solder.

206. (previously presented) The chip package in claim 197 further comprising a substrate under said die and under said first and second portions.

207. (previously presented) The chip package in claim 206, wherein said substrate comprises silicon.

208. (currently amended) The chip package in claim 197 further comprising a filter over said second ~~polymer~~ insulating layer.